CLAIMS

1. A method of forming a memory cell comprising:

providing a semiconductor substrate;

forming a P well in said semiconductor substrate;

forming an N well in said semiconductor substrate adjacent to said P well;

forming an N type active region in said P well;

forming a P type active region in said N well;

forming an isolation region in said semiconductor substrate to isolate said N type active region from said P type active region;

providing a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer over said N type active region and a P+ polysilicon layer over said P type active region; and

forming a diffusion barrier layer in said polysilicide gate electrode structure over a portion of said polycrystalline silicon film between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film.

2. A method of forming a memory cell comprising:

providing a semiconductor substrate;

forming a P well in said semiconductor substrate;

forming an N well in said semiconductor substrate;

forming an NMOS transistor having an N type active region in said P well;

forming a PMOS transistor having a P type active region in said N well;

forming an isolation region in said semiconductor substrate to isolate said N type active region from said P type active region;

providing a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said NMOS transistor and a P+ polysilicon layer forming a portion of said PMOS transistor; and

forming an oxide diffusion barrier layer in said polysilicide gate electrode structure over a portion of said polycrystalline silicon film between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film.

3. A method of forming a memory cell comprising:

providing a semiconductor substrate;

forming a P well in said semiconductor substrate;

forming an N well in said semiconductor substrate;

forming an NMOS transistor having an N type active region in said P well;

forming a PMOS transistor having a P type active region in said N well;

forming an isolation region in said semiconductor substrate to isolate said N type active region from said P type active region;

providing a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said NMOS transistor and a P+ polysilicon layer forming a portion of said PMOS transistor; and

forming an oxide diffusion barrier layer in said polysilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film, wherein said polysilicide gate electrode structure and said oxide diffusion barrier layer are arranged such that migration of P+ dopants from said P+ polysilicon layer to said overlying metal, metal silicide, or metal nitride film is impeded by said diffusion barrier layer.

4. A method of forming a memory cell comprising:

providing a semiconductor substrate;

forming a P well in said semiconductor substrate;

forming an N well in said semiconductor substrate;

forming an NMOS transistor having an N type active region in said P well;

forming a PMOS transistor having a P type active region in said N well;

forming an isolation region in said semiconductor substrate to isolate said N type active region from said P type active region;

providing a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said NMOS transistor and a P+ polysilicon layer forming a portion of said PMOS transistor; and

forming an oxide diffusion barrier layer formed in said polysilicide gate electrode structure over a substantial portion of said P+ polysilicon layer between said P+ polysilicon layer and said metal, metal silicide, or metal nitride film, wherein said oxide diffusion barrier layer does not extend over a portion of said N+ polysilicon layer.

5. A method of forming a memory cell comprising:

providing a semiconductor substrate;

forming a P well in said semiconductor substrate;

forming an N well in said semiconductor substrate;

forming an NMOS transistor having an N type active region in said P well;

forming a PMOS transistor having a P type active region in said N well;

forming an isolation region in said semiconductor substrate to isolate said N type active region from said P type active region;

providing a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said NMOS transistor and a P+ polysilicon layer forming a portion of said PMOS transistor; and

forming an oxide diffusion barrier layer formed in said polysilicide gate electrode structure over a portion of said P+ polysilicon layer between said P+ polysilicon layer and said metal, metal silicide, or metal nitride film, wherein said oxide diffusion barrier layer is arranged such that said metal, metal silicide, or metal nitride film defines an N type common boundary with said N+ polysilicon layer that is larger than a P type common boundary defined by said metal, metal silicide, or metal nitride film and said P+ polysilicon layer.

6. A method of forming a memory cell comprising:

providing a semiconductor substrate;

forming a P well in said semiconductor substrate;

forming an N well in said semiconductor substrate;

forming an NMOS transistor having an N type active region in said P well;

forming a PMOS transistor having a P type active region in said N well;

forming an isolation region in said semiconductor substrate to isolate said N type active region from said P type active region;

providing a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said NMOS transistor and a P+ polysilicon layer forming a portion of said PMOS transistor; and

forming an oxide diffusion barrier layer formed in said polysilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film, wherein said polysilicide gate electrode structure and said diffusion barrier layer are arranged such that migration of N+ dopants from said N+ polysilicon layer to said overlying metal, metal silicide, or metal nitride film is impeded by said diffusion barrier layer.

7. A method of forming a memory cell comprising:

providing a semiconductor substrate;

forming a P well in said semiconductor substrate;

forming an N well in said semiconductor substrate;

forming an NMOS transistor having an N type active region in said P well;

forming a PMOS transistor having a P type active region in said N well;

forming an isolation region in said semiconductor substrate to isolate said N type active region from said P type active region;

providing a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline

silicon film comprises an N+ polysilicon layer forming a portion of said NMOS transistor and a P+ polysilicon layer forming a portion of said PMOS transistor; and

forming an oxide diffusion barrier layer formed in said polysilicide gate electrode structure over a portion of said N+ polysilicon layer between said N+ polysilicon layer and said metal, metal silicide, or metal nitride film, wherein said diffusion barrier layer does not extend over a portion of said P+ polysilicon layer.

8. A method of forming a memory cell comprising:

providing a semiconductor substrate;

forming a P well in said semiconductor substrate;

forming an N well in said semiconductor substrate;

forming an NMOS transistor having an N type active region in said P well;

forming a PMOS transistor having a P type active region in said N well;

forming an isolation region in said semiconductor substrate to isolate said N type active region from said P type active region;

providing a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said NMOS transistor and a P+ polysilicon layer forming a portion of said PMOS transistor; and

forming an oxide diffusion barrier layer formed in said polysilicide gate electrode structure over a portion of said N+ polysilicon layer between said N+ polysilicon layer and said metal, metal silicide, or metal nitride film, wherein said oxide diffusion barrier layer is arranged such that said metal, metal silicide, or metal nitride film defines a P type common boundary with said P+ polysilicon layer that is larger than an N type common boundary defined by said metal, metal silicide, or metal nitride film and said N+ polysilicon layer.

9. A method of forming a memory cell comprising:

providing a semiconductor substrate;

forming a P well in said semiconductor substrate;

forming an N well in said semiconductor substrate;

forming an NMOS transistor having an N type active region in said P well;

forming a PMOS transistor having a P type active region in said N well;

forming an isolation region in said semiconductor substrate to isolate said N type active region from said P type active region;

providing a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said NMOS transistor and a P+ polysilicon layer forming a portion of said PMOS transistor; and

forming an oxide diffusion barrier layer formed in said polysilicide gate electrode structure over said N+ polysilicon layer and said P+ polysilicon layer between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film, wherein said polysilicide gate electrode structure and said diffusion barrier layer are arranged such that

migration of P+ dopants from said P+ polysilicon layer to said overlying metal, metal silicide, or metal nitride film is impeded by said diffusion barrier layer and

migration of N+ dopants from said N+ polysilicon layer to said overlying metal, metal silicide, or metal nitride film is impeded by said diffusion barrier layer.

10. A method of forming an SRAM memory cell comprising:

providing a semiconductor substrate;

forming a P well in said semiconductor substrate;

forming an N well in said semiconductor substrate;

forming a flip-flop having two access transistors and a pair of cross coupled inverters, wherein each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor, and wherein said pull-up transistor defines a P type active region in said N well and said pull-down transistor defines an N type active region in said P well;

forming an isolation region in said semiconductor substrate to isolate said N type active region from said P type active region;

providing a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said pull-down transistor and a P+ polysilicon layer forming a portion of said pull-up transistor; and

forming an oxide diffusion barrier layer in said polysilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film over a portion of said polycrystalline silicon film.

11. A method of forming an SRAM memory cell comprising:

providing a semiconductor substrate;

forming a P well in said semiconductor substrate;

forming an N well in said semiconductor substrate;

forming a flip-flop having two access transistors and a pair of cross coupled inverters, wherein each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor, and wherein said pull-up transistor defines a P type active region in said N well and said pull-down transistor defines an N type active region in said P well;

forming an isolation region in said semiconductor substrate to isolate said N type active region from said P type active region;

providing a polysilicide gate electrode structure composed of a polycrystalline silicon film having a thickness of between about 500 Å and about 4000 Å and an overlying metal, metal silicide, or metal nitride film having a thickness of between about 500 Å and 4000 Å, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said pull-down transistor and a P+ polysilicon layer forming a portion of said pull-up transistor; and

forming an oxide diffusion barrier layer having a thickness of between about 3 Å and about 125 Å formed in said polysilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film over a portion of said polycrystalline silicon film.

12. A method of forming an SRAM memory cell comprising:

providing a semiconductor substrate;

forming a P well in said semiconductor substrate;

forming an N well in said semiconductor substrate;

forming a flip-flop having two access transistors and a pair of cross coupled inverters, wherein each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor, and wherein said pull-up transistor defines a P type active region in said N well and said pull-down transistor defines an N type active region in said P well;

forming an isolation region in said semiconductor substrate to isolate said N type active region from said P type active region;

providing a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said pull-down transistor and a P+ polysilicon layer forming a portion of said pull-up transistor; and

forming an oxide diffusion barrier layer formed in said polysilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film over a portion of said N+ polysilicon layer and said P+ polysilicon layer.

13. A method of forming an SRAM memory cell comprising:

providing a semiconductor substrate;

forming a P well in said semiconductor substrate;

forming an N well in said semiconductor substrate;

forming a flip-flop having two access transistors and a pair of cross coupled inverters, wherein each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor, and wherein said pull-up transistor defines a P type active region in said N well and said pull-down transistor defines an N type active region in said P well;

forming an isolation region in said semiconductor substrate to isolate said N type active region from said P type active region;

providing a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said pull-down transistor and a P+ polysilicon layer forming a portion of said pull-up transistor; and

forming an oxide diffusion barrier layer formed in said polysilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film, wherein said polysilicide gate electrode structure and said diffusion barrier layer are arranged such that migration of P+ dopants from said P+ polysilicon layer to said overlying metal, metal silicide, or metal nitride film is impeded by said diffusion barrier layer.

14. A method of forming an SRAM memory cell comprising:

providing a semiconductor substrate;

forming a P well in said semiconductor substrate;

forming an N well in said semiconductor substrate;

forming a flip-flop having two access transistors and a pair of cross coupled inverters, wherein each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor, and wherein said pull-up transistor defines a P type active region in said N well and said pull-down transistor defines an N type active region in said P well;

froming an isolation region in said semiconductor substrate to isolate said N type active region from said P type active region;

providing a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said pull-down transistor and a P+ polysilicon layer forming a portion of said pull-up transistor; and

forming an oxide diffusion barrier layer in said polysilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film, wherein said polysilicide gate electrode structure and said diffusion barrier layer are arranged such that migration of N+ dopants from said N+ polysilicon layer to said overlying metal, metal silicide, or metal nitride film is impeded by said diffusion barrier layer.

15. A method of forming a memory cell array comprising a plurality of SRAM cells arranged in rows and columns, wherein each cell of said array is connected to a word line and to a pair of bit lines, said method comprising:

providing a semiconductor substrate;

forming a P well in said semiconductor substrate;

forming an N well in said semiconductor substrate;

forming a flip-flop having two access transistors and a pair of cross coupled inverters, wherein each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor, and wherein said pull-up transistor defines a P type active region in said N well and said pull-down transistor defines an N type active region in said P well;

forming an isolation region in said semiconductor substrate to isolate said N type active region from said P type active region;

providing a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said pull-down transistor and a P+ polysilicon layer forming a portion of said pull-up transistor; and

forming an oxide diffusion barrier layer formed in said polysilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film over a portion of said polycrystalline silicon film.

16. A method of fabricating an SRAM memory cell, said method comprising:

providing a semiconductor substrate;

forming a P well in said semiconductor substrate;

forming an N well in said semiconductor substrate;

providing a flip-flop including two access transistors and a pair of cross coupled inverters, wherein each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor, and wherein said pull-up transistor defines a P type active region in said N well and said pull-down transistor defines an N type active region in said P well;

arranging an isolation region to isolate said N type active region from said P type active region;

providing a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said pull-down transistor and a P+ polysilicon layer forming a portion of said pull-up transistor; and

forming a diffusion barrier layer in said polysilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film over a substantial portion of said polycrystalline silicon film.

17. A method of fabricating an SRAM memory cell, said method comprising:

providing a semiconductor substrate;

forming a P well in said semiconductor substrate;

forming an N well in said semiconductor substrate;

forming a P type active region of a pull-up transistor in said N well;

forming a gate oxide layer and a conductive gate of said pull-up transistor over said P type active region;

forming an N type active region of a pull-down transistor in said P well;

forming a gate oxide layer and a conductive gate of said pull-down transistor over said N type active region;

forming an isolation region between said N type active region and said P type active region;

forming a polycrystalline silicon film over said pull-down transistor and said pull-up transistor;

doping selectively said polycrystalline silicon film to form an N+ polysilicon layer over said pull-down transistor and a P+ polysilicon layer over said pull-up transistor;

forming a diffusion barrier layer over a substantial portion of said polycrystalline silicon film; and

forming a metal, metal silicide, or metal nitride film over said doped polycrystalline silicon film and said diffusion barrier layer.

18. A method of fabricating a memory cell array by arranging a plurality of said SRAM cells in rows and columns and connecting each SRAM cell of said array to a word line and to a pair of bit lines, wherein each of said SRAM cells is fabricated by:

providing a semiconductor substrate;

forming a P well in said semiconductor substrate;

forming an N well in said semiconductor substrate;

providing a flip-flop including two access transistors and a pair of cross coupled inverters, wherein each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor, and wherein said pull-up transistor defines a P type active region in said N well and said pull-down transistor defines an N type active region in said P well;

arranging an isolation region to isolate said N type active region from said P type active region;

providing a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said pull-down transistor and a P+ polysilicon layer forming a portion of said pull-up transistor; and

forming a diffusion barrier layer in said polysilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film over a substantial portion of said polycrystalline silicon film.

19. A method of fabricating a computer system by arranging a microprocessor in communication with a memory cell array via a data communication path and fabricating said memory cell array by arranging a plurality of said SRAM cells in rows and columns and connecting each SRAM cell of said array to a word line and to a pair of bit lines, wherein each of said SRAM cells is fabricated by:

providing a semiconductor substrate;

forming a P well in said semiconductor substrate;

forming an N well in said semiconductor substrate;

providing a flip-flop including two access transistors and a pair of cross coupled inverters, wherein each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor, and wherein said pull-up transistor defines a P type active region in said N well and said pull-down transistor defines an N type active region in said P well;

arranging an isolation region to isolate said N type active region from said P type active region;

providing a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said pull-down transistor and a P+ polysilicon layer forming a portion of said pull-up transistor; and

forming a diffusion barrier layer in said polysilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film over a substantial portion of said polycrystalline silicon film.

20. The method as claimed in claim 1 wherein said diffusion barrier layer comprises an ultrathin oxide diffusion barrier layer.

21. The method as claimed in claim 1 wherein said diffusion barrier layer comprises an ultrathin diffusion barrier layer.

22. The method as claimed in claim 21 wherein said ultrathin diffusion barrier layer has a thickness of less than 125 Å.

23. The method as claimed in claim 21 wherein said ultrathin diffusion barrier layer has a thickness of between about 10 Å and about 15 Å.

24. The method as claimed in claim 21 wherein said ultrathin diffusion barrier layer has a thickness of between about 3 Å and about 125 Å.

25. The method as claimed in claim 21 wherein said ultrathin diffusion barrier layer has a thickness of between about 3 Å and about 50 Å.

26. The method as claimed in claim 21 wherein said ultrathin diffusion barrier layer has a thickness of between about 3 Å and about 125 Å and said polycrystalline silicon film has a thickness of between about 500 Å and about 4000 Å.

27. The method as claimed in claim 5 wherein metal, metal silicide, or metal nitride film form defines an overcoated portion of said P+ polysilicon layer and wherein said diffusion barrier layer is formed in said polysilicide gate electrode structure between said metal, metal silicide, or metal nitride film and said P+ polysilicon layer over the entire extent of said overcoated portion of said P+ polysilicon layer.

28. The method as claimed in claim 8 wherein metal, metal silicide, or metal nitride film form defines an overcoated portion of said N+ polysilicon layer and wherein said diffusion barrier layer is formed in said polysilicide gate electrode structure between said metal, metal silicide, or metal nitride film and said N+ polysilicon layer over the entire extent of said overcoated portion of said N+ polysilicon layer.

29. The method of fabricating an SRAM memory cell as claimed in claim 17 wherein said diffusion barrier layer is formed by selective chemical oxidation of said polycrystalline silicon film.

30. The method of fabricating an SRAM memory cell as claimed in claim 17 wherein said diffusion barrier layer is formed by silicon nitride deposition.

31. A method of forming a gate electrode structure for a semiconductive device having N type and P type active regions, said method comprising:

forming a film having an N+ polysilicon layer over the N type active region and a P+ polysilicon layer over the P type active region;

forming an oxide layer over a portion of said film; and

providing a metal, metal silicide, or metal nitride film on said film and said oxide layer.

32. The method as claimed by claim 31 wherein said oxide layer is formed over said N+ and P+ polysilicon layers.

33. The method as claimed by claim 31 wherein said oxide layer is formed over said N+ polysilicon layer.

34. The method as claimed by claim 31 wherein said oxide layer is formed over said P+ polysilicon layers.

35. The method as claimed by claim 31 wherein said N+ polysilicon layer forms a portion of a pull-down transistor and said P+ polysilicon layer forms a portion of a pull-up transistor, and said oxide layer is formed over said N+ and P+ polysilicon layers.

36. The method as claimed by claim 31 wherein said N+ polysilicon layer forms a portion of a pull-down transistor, and said oxide layer is formed over said N+ polysilicon layer.

37. The method as claimed by claim 31 wherein said P+ polysilicon layer forms a portion of a pull-up transistor, and said oxide layer is formed over said P+ polysilicon layer.

38. The method as claimed by claim 31 wherein said oxide layer is silicon dioxide.

39. The method as claimed by claim 31 wherein said oxide layer has a thickness under 125 Å.

40. A method of forming a memory cell comprising:

providing a semiconductor substrate;

forming a P well in said semiconductor substrate;

forming a N well in said semiconductor substrate adjacent to said P well;

forming a N type active region in said P well;

forming a P type active region in said N well;

forming an isolation region arranged to isolate said N type active region from said P type active region; and

forming a gate electrode structure having a film with an N+ polysilicon layer over said N type active region and a P+ polysilicon layer over said P type active region, an oxide layer formed over a portion of said film, and a metal, metal silicide, or metal nitride film overlaying said film and said oxide layer.